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## ETHERTON LAW GROUP LLC

5555 EAST VAN BUREN STREET  
SUITE 100  
PHOENIX, AZ 85008TEL: 602-681-3331  
FAX: 602-681-3339**To:** United States Patent and Trademark Office  
Central Facsimile**Fax:** 571-273-8300**Phone:****Re:** Request for Interview**Appl. No:** 10/697406**Atty File:** 52003218 (ELG 439-002)**FROM:** Sandra L. Etherton, Reg. No. 36,982**FAX:** 602-681-3339**PHONE:** 602-681-3331**PAGES:** 3 including cover**DATE:** Sept 21, 2007

\* RE-SENT \*

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*In re Application of*

**Applicants:** Guenther, et al.  
**Title of Invention:** Method for Improving Performance of Critical Path in Field Programmable Gate Arrays  
**Filed:** 10/29/2003  
**Serial Number:** 10/697,406  
**Atty Docket No.:** 52003218

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## CERTIFICATE OF TRANSMISSION under 37 CFR §1.8 and 1.6(d)

I hereby certify that this correspondence is being transmitted by facsimile on the date indicated below to the central facsimile number: 571-273-8300.

  
Sandra L. Etherton

Date 9/21/07

**Applicant-Initiated Request for Interview**

Mail Stop AF  
Commissioner of Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Dear Sir:

Pursuant to MPEP §713, the Applicants' attorney and agent of record request a telephonic interview with the Examiner on Tuesday, September 25, 2007 at 11:00 a.m., Arizona time (2:00 pm in Virginia) regarding the above-identified application. In addition to the Examiner, the expected participants are Sandra L. Etherton, Attorney for Applicant, and Russell W. Guenther, first-named inventor and Agent for Applicant.

**Intended Purpose and Content**

All claims in the pending application have been finally rejected under §102 over Togawa. The issue to be discussed is that Togawa discloses a fundamentally different invention from that claimed in the present application. Applicants believe clarifying what Togawa discloses will render the rejections moot.

439-002

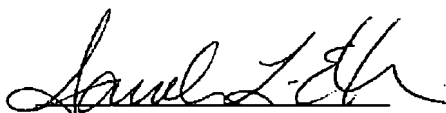
Applicant-Initiated Request for Interview  
SN 10/697,406

Specifically, Togawa minimizes *crossings* between chips (or if applying that same idea to one chip, then crossings between clusters of logic located physically close to each other). In contrast, the present invention minimizes the *physical routing distance* in the physical implementation of a logic path. The mechanism disclosed in the present invention for achieving the optimization of the physical distance is totally different in concept and implementation than the partitioning thoughts of Togawa.

If the date and time set forth above is acceptable to the Examiner, Applicants' representatives will call the Examiner at 571-272-1906 at the appointed time. If the date and time are not acceptable to the Examiner, the Examiner is welcome to propose a new date and time.

Respectfully submitted,

9/21/07  
Dated



Sandra L. Etherton  
Registration No. 36,982  
Tel: 602-681-3331

Russell W. Guenthner  
Registration No. 54,140  
Tel: 602-862-5479

Bull HN Information Systems Inc.  
MS B55  
13430 North Black Canyon Highway  
Phoenix, AZ 85029